CLAIMS

1. A rate matching circuit for adjusting the number of bits in a data block, the data block comprising a plurality of interleaved words generated by the action of an interleaving circuit on a coded output generated by the action of a coding circuit on a digital input, the coded output having a greater number of bits than the digital input, the rate matching circuit having means for adjusting the number of bits in the data block using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel, characterised in that means are provided for selecting the rate matching pattern depending on the characteristics of the coding circuit and of the interleaving circuit.

2. A rate matching circuit as claimed in claim 1, characterised in that the rate matching pattern is selected in such a way that all bits of the digital input can be derived from the remainder of the bits in successive interleaved blocks.

3. A rate matching circuit as claimed in claim 1 or 2, characterised in that the rate matching pattern for each interleaved word within the data block is offset with respect to the adjacent interleaved word or words within the block.

4. A rate matching circuit as claimed in any one of claims 1 to 3, characterised in that the rate matching pattern is selected as a function of the interleaving depth of the interleaving circuit.

5. A coding device comprising a rate matching circuit as claimed in any one of claims 1 to 4, further comprising an interleaving circuit and a coding circuit.

6. A decoding device comprising for decoding a signal coded by a coding device as claimed in claim 5, and comprising a data reconstruction circuit for reconstructing the interleaved words, a de-interleaving circuit and a channel decoder.

7. A communication system comprising a transmitter having a coding device as claimed in claim 5, and a receiver having a decoding device as claimed in claim 6.

8. A system as claimed in claim 7, comprising a plurality of coding devices, each for coding a respective digital input, and a multiplexer for combining output data words of the coding devices for subsequent transmission by the transmission system on a single transmission channel.

9. A system as claimed in claim 8, wherein the outputs of different coding devices are selected to have different data rates, the combined data rate corresponding to the channel capacity of the transmission channel.

10. A method of operating a rate matching circuit to adjust the number of bits in a data block, the data block comprising a plurality of interleaved words generated by the action of an interleaving circuit on a coded output generated by the action of a coding circuit on a digital input, the coded output having a greater number of bits than the digital input, the rate matching circuit adjusting the number of bits in the data block using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel, characterised by selecting the rate matching pattern depending on the characteristics of the coding circuit and of the interleaving circuit.